REMARKS

The Examiner objected to the Abstract. Applicant has canceled the Abstract as filed and submitted herewith a replacement Abstract.

Minor amendments have been made to some of the claims to emphasize that the true/complement nodes of the latch are the latch nodes (as opposed to some other nodes). No new matter has been added, and it is further submitted that these amendments clarify but do not narrow the scope of the claimed invention.

Claims 1-2 were rejected under 35 U.S.C. 102(b) as being anticipated by Seki. These claims have been canceled.

Claims 9-11, 14-18, 21-22, 25 and 28 were rejected under 35 U.S.C. 102(b) as being anticipated by Sakata. Applicant respectfully traverses.

Turning first to claim 9, Applicant claims a data latch having a true and complement latch nodes, along with control circuitry responsive to a control signal for shorting those two latch nodes together. The Examiner points to Sakata Figure 1. Sakata teaches a memory cell 100 having supply nodes S1 and S2. The data latch for the cell 100 includes a true latch node S3 and a complement latch node S4. Switching circuitry formed from CMOS switches 201-207 functions responsive to control signals in order to selectively apply reference voltages (Vdd/Gnd) to the supply nodes S1 and S2. In one mode of operation, the CMOS switches 201-207 will cause a ground voltage (Gnd) to be applied to both of the supply nodes S1 and S2. This, according to the Examiner, effectively shorts the nodes S1 and S2 together.

With respect to claim 9, however, Applicant claims shorting of the true and complement latch nodes of the latch together (see, Specification Figure 3). This would be equivalent to

shorting the latch nodes S3 and S4 in Sakata. Contrary to the Examiner's position, because of the presence of resistances R1/R2, the CMOS switches 201-207 do not function in any way to short latch nodes S3 and S4 together as is claimed by Applicant. Accordingly, there is no anticipation of claim 9 by Sakata. Applicant respectfully submits that claim 9, along with its dependent claims 10-13 are patentable over Sakata.

Turning next to claim 14, Applicant claims first and second pass gates coupling the true/complement latch nodes to the true/complement bit lines, respectively. Applicant further claims that the control signal is applied to activate these pass gate thus shorting the true/complement latch nodes to their respective bit lines so as to clear the data latch. Sakata shows first and second pass gates N1 and N2 with a wordline WL control signal. There is no teaching or suggest in Sakata for activating the WL control signal (other than in the normal read/write operations) to short the true/complement latch nodes S3/S4 to the bit lines in the manner claimed to destroy the stored data. In fact, the teaching in Sakata is to the opposite. At col. 3, lines 6-7 and lines 24-25, Sakata specifically teaches bringing the word line WL into a non-selected state so that the pass transistors N1 and N2 are turned off. No teaching or suggestion in made in Sakata for the claimed data destroying operation with an activated WL. Applicant respectfully submits that claim 14, along with its dependent claim 15, are patentable over Sakata.

In claim 16, Applicant claims circuitry for shorting one of the true/complement latch nodes to a reference voltage in order to destroy stored data. Again, the Examiner appears to point to supply nodes S1 and S2. As discussed above, however, the supply nodes are not the same thing as the claimed true/complement latch nodes of the latch. Those latch nodes, in

Sakata, are latch nodes S3 and S4. There is no teaching or suggestion in Sakata for any circuitry operable to short one of latch nodes S3/S4 to a reference voltage to achieve data destruction. Rather, the operation of Sakata merely controls application of a reference voltage to nodes S1/S2. Since nodes S1/S2 are coupled to nodes S3/S4 through resistances R1/R2, respectively, there is no structure provided for enabling a short between a reference voltage at nodes S1/S2 and one or more of the latch nodes S3/S4. Applicant respectfully submits that claim 16, along with its dependent claims 17-20, are patentable over Sakata.

Turning next to claim 21, Applicant claims circuitry for shorting both of the true/complement latch nodes to a reference voltage in order to destroy stored data. Again, for at least the same reasons discussed above, Sakata fails to teach or suggest the claimed circuitry. There is no teaching or suggestion in Sakata for shorting both latch nodes S3/S4 to a reference voltage. Resistances R1/R2 exist between nodes S1/S2 and latch nodes S3/S4 thus precluding a shorting from occurring. Applicant respectfully submits that claim 21, along with its dependent claims 22-30, are patentable over Sakata.

Claims 3-6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Seki in view of Murray. These claims have been canceled.

Claims 7-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Seki in view of Sakata. These claims have been canceled.

Claims 12-13, 19-20 and 29-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata in view of Murray and Itoh. Applicant respectfully traverses and submits that these claims are patentable over the cited art for at least the same reasons as their respective independent claims. Neither Murray nor Itoh address the deficiencies noted above

with respect to a) shorting of the true and complement latch nodes of the latch together (claim 9), b) shorting one of the true/complement latch nodes to a reference voltage (claim 16), or c) shorting both of the true/complement latch nodes to a reference voltage (claim 21). As discussed above, Sakata fails to teach or suggest shorting either or both of latch nodes S3/S4 in the manner claimed by Applicant. Similarly, in Murray there is no teaching for shorting the latch nodes 114/116 in the manner claimed by Applicant. Finally, in Itoh, there is no teaching for shorting the latch nodes N1/N2 in the manner claimed by Applicant.

Claims 23-24 and 26-27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata in view of Matsui. Applicant respectfully traverses and submits that these claims are patentable over the cited art for at least the same reasons as their respective independent claims. Matsui fails to address the deficiencies noted above with respect to shorting both of the true/complement latch nodes to a reference voltage (claim 21). As discussed above, Sakata fails to teach or suggest shorting either or both of latch nodes S3/S4 in the manner claimed by Applicant. Similarly, in Matsui there is no teaching for shorting the latch nodes N1/N2 in the manner claimed by Applicant.

Claims 31-34 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata in view of Yanigisawa. These claims have been canceled.

Claims 35-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over Murray in view of Casper and Brady. Applicant respectfully traverses.

The Examiner correctly concedes that Murray fails to teach circuitry that shorts a bit line to a reference voltage. The Examiner relies on Casper to meet this limitation. It is the Examiner's position that Casper teaches shorting a word line to a bit line. This is not correct.

What Casper recognizes is that fabrication defects might arise, and that one such defect would be a short between a bit line and a word line (col. 2, lines 13-16). Such a short is not a purposefully created circuit structure. A review of Casper Figure 2 clearly shows no circuit structure for effectuating the bit line to word line short. Still further, there is no teaching in Casper for one being able to exercise control over when this fabrication defect short occurs, such that it can be controlled to occur "while the pass gate is activated" and in response to a control signal as is specifically claimed by Applicant. The potential occurrence of a fabrication error to create a bit/word line short simply does not give rise to a teaching which meets the specifically recited claim language for circuitry that operates, responsive to a control signal, to short the bit line to a reference voltage. It does not matter that such a fabrication error bit/word line short may have the same effect as a bit line/reference voltage short because the existence of the fabrication error short in Casper is not purposeful and does not occur responsive to a control signal. Applicant accordingly submits that the Examiner has failed to make out the prima facie case for rejection of claim 35. The cited prior art combination fails to teach or suggest each claim limitation. Applicant respectfully submits that claim 35, along with its dependent claims 36-39, are patentable over the prior art.

In view of the foregoing, Applicant respectfully submits that the pending claims are in condition for favorable action and allowance.

Respectfully submitted,
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